a third region of a second conductivity type over said second region, said second and third regions forming a junction;

a fourth region of said first conductivity type over said third region;

a trench through said fourth and third regions; and

a gate in said trench; wherein a deepest part of said third region is laterally spaced from said trench; and wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.

53. A transistor as in claim 42 wherein the ~~said~~ deepest part of said third region is doped heavier than a part of said third region which ~~part~~ is adjacent said trench.

REMARKS

Claims 17-29 are pending. Claims 30-53 are newly presented.

In an office action of the Parent Application, mailed on June 8, 1994, the Examiner rejected Claims 17-29 under 35 U.S.C. § 103 over Tonnel (U.S. Patent 4,420,379), stating:

> [With respect to Claim 17, a] peripheral cell shown in Figure 3 includes at least one trench extending into epitaxial layer (21) to a finite depth, d1, source regions (26) formed in a body region portion (25) that extends a finite depth, d2, at one location, whereby the body region includes a peripheral portion (22) at another location extending a finite depth, d3. Examining cross-section profile shown in Figure 12, we find that, as opposed to the rendering of Figure 3, Tonnel fully expected that the each of d1 and d2 to be less than d3, that d1 exceeds d2 and that a distance between either trench and either peripheral body region (22) exceed a distance between either trench and an adjacent body portion region

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(25). We thus conclude it to have been obvious for one to have accordingly disposed the regions, portions and trenches of the Figure 3 embodiment.

In re Claims 22 and 23, evidently from Figures 3 and 12, Tonnel expected a DMOS cell to possess two trenches with each trench having four sides.

In re Claim 28, evidently from Figure 3, Tonnel expected a DMOS cell to include two parallel trenches having finite dimensions, thus obviously rendering an open cell configuration.

In re Claim 27, Tonnel expected to physically and electrically tie the trenches together with peripheral ring electrode (24) obviously rendering the claimed close cell configuration.

In response to this office action of June 8, 1994, Applicants submitted remarks on September 30, 1994:

Applicants respectfully traverse the Examiner's rejection of Claims 17-29 over Tonnel. Specifically, Tonnel does not disclose a trench DMOS transistor, as recited in each of Claims 17-29, but a VMOS transistor. Further, there is no teaching in Tonnel's detailed description regarding the relative depths of the various structures in Tonnel's Figs. 4-19. (See Tonnel's specification, beginning at col. 4, line 5 to col. 6, line 36, where neither the depth of the slot 30, nor the depth of P type region 22 is given). In fact, as the Examiner pointed out, Tonnel's Figs. 4-19 contradict the structure in Fig. 3: whereas the P type body region in Fig. 3 is shown to be of a lesser depth than the depth of slot 30, the corresponding P type body region in Figs. 4-19 are shown to have a greater depth than slot 31. Since Tonnel's Figs 4-19 are provided to illustrate the manufacturing process for the structure of Fig. 3 (Tonnel's col. 4, lines 5-7), such contradiction clearly indicates that the relative depths of structures shown in Figs. 4-19 are not drawn to scale and are merely fortuitous. Thus, Tonnel does not appreciate, and therefore does not teach or suggest, the structures recited in Applicants' Claims 17-29 and their significance. Hence, Tonnel is not an enabling reference, neither disclosing nor suggesting Applicants' Claims 17-29 to one of ordinary skill in the art. To be an effective reference, it is required that "the prior art reference must be enabling, thus placing the alleged disclosed matter in the possession of the public". Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1 USPQ2d 1241. Because Tonnel is not an enabling disclosure, withdrawal

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> of the Examiner's rejection under 35 U.S.C. § 103, reconsideration, and allowance of Claims 17-29 are requested.

In response to Applicants' remarks, the Examiner stated in the final office action of the Parent Application, mailed on December 29, 1994:

> On page 2 the Applicants, in the same vein, choose to hold that our characterization of Tonnel as showing a trench DMOS transistor is incorrect. The Applicants characterize the Tonnel device instead as a VMOS transistor.
>
> In response, we believe that both characterizations are consistent with the Tonnel transistor. The Applicants' VMOS terminology indicates a substantial Vertical current path in the Metal Oxide Semiconductor (VMOS) transistor; and our trench DMOS terminology indicates that Tonnel formed insulated gate electrode (32) within a trench etched into semiconductor substrate material (21) whereby the transistor was constructed in a vertical Diffused manner. Hence the "D" component of the DMOS acronym. Tonnel chose to characterize as slots (30) whereas we chose to synnomously characterize slots (30) instead as trenches to emphasize our point of view that the Tonnel trench DMOS transistor falls well within the scope of Applicants' Claim 17. We presently find that our characterization of the Tonnel transistor is entirely consistent with DMOS terminology as used by Blanchard '535, Reference AA presently provided by the Applicants. We thus conclude therefrom that the Applicants' traverse of our characterization of the Tonnel transistor as a trench DMOS transistor has little and insufficient merit - especially in view of the fact that VMOS terminology constitutes a mere distinction without any difference whatsoever.

Applicants respectfully submit that the Examiner is in error. Tonnel, rather than Applicants, characterizes the transistor shown in Tonnel's Fig. 3 as a "VMOS transistor" (Col. 2, lines 27-30):

> Fig. 3 shows, in a sectioned perspective view, a power V-MOS transistor structure that is to be manufactured by the process in accordance with the present invention.

Tonnel defines the term "VMOS" at col. 1, lines 19-24:

> "V-MOS" indicates a MOS with V-shaped slots and "U-MOS" one with U-shaped ones.

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> These V-MOS and U-MOS transistors operate vertically or roughly vertically and may be used in particular applications in which relatively high voltages are applied and relatively high currents flow.

Therefore, the Examiner mistakenly characterized Tonnel's VMOS transistor as "consistent with" a trench DMOS transistors. In fact, Tonnel clearly teaches that what distinguishes a "V-MOS" transistor from other transistors of vertical current paths is the shape of the slot. In this instance, the "V" shape of the VMOS transistor significantly distinguishes it from a trench DMOS transistor. In particular, the "V" shape concentrates electric field lines so as to cause crowding of current paths at the vertex of the "V" at which breakdown can occur. This current path crowding effect is clearly shown in Figure 5 of "Optimization of Nonplanar Power MOS Transistors" by Lisiak, which the Examiner cited as "a measure of ordinary skill". The present invention seeks to specifically avoid such a breakdown at the trench of a trench DMOS transistor (Applicants' Specification at page 9, lines 9-32). Thus, one of ordinary skill seeking to avoid breakdown at the trench would not be motivated to modify Tonnel in the direction of the present invention. Hence, Tonnel teaches away from the present invention. Accordingly, Applicants 17-29 are not obvious from the teaching of Tonnel.

The Examiner's remaining comments regarding Tonnel based on the teaching of Lisiak are inapposite since the Examiner is rejecting Applicants' Claims 17-29 under 35 U.S.C. § 103 based on Tonnel only and not based on the combined teachings of Tonnel and Lisiak. Further, the Examiner has not shown how the combined teachings of Tonnel and Lisiak discloses or suggests Applicants' Claims 17-29. The Examiner merely speculated that the disclosed device dimensions in Lisiak and Tonnel are not inconsistent with each other. The combined teachings of Lisiak and Tonnel, however, thus fall short of providing support for the Examiner's conclusion that "one of ordinary skill at the

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time of Tonnel would have understood Tonnel as clearly, unambiguously and deliberately disclosing at least a structure fully consistent with the Invention claimed". The discrepancies between Tonnel's Fig.3 and Tonnel's Figs. 4-12, which are provided to show the steps for manufacturing the structure of Fig. 3 (Tonnel's col. 4, lines 5-7), clearly refute the Examiner's conclusion.

In the final office action of the Parent Application, the Examiner also maintained his rejection under the judicially established doctrine of obviousness-type double patenting, citing Tonnel. For the reasons set forth above, Applicants respectfully submit that Applicants Claims 17-19 are patentable over U.S. Patent 5,072,266's Claim 2 and its dependent claims, considered in conjunction with Tonnel.

Newly presented Claims 30-53 are believed to be patentable over the prior art references of record.

For the foregoing reasons, Applicants believe that all claims (i.e. Claims 17-53) are allowable and respectfully request their allowance. If the Examiner has any questions regarding the above, the Examiner is respectfully requested to telephone the undersigned Attorney at 408-453-9200.

Respectfully submitted,

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